This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2019.2908243, IEEE Transactions on Circuits and Systems II: Express Briefs

Energy-Efficient Nonvolatile SRAM Design Based on Resistive Switching Multi-Level Cells

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***Abstract*—A new nonvolatile Static Random Access Memory (nvSRAM) design based on the multi-level cell (MLC) characteristics of resistive RAMs (RRAMs) is presented in this brief to reduce the store energy of frequent-off and instant-on applications. The data store circuitry is designed to enable the energy-efficient multi-bit data backup of every two SRAM cells into a single four-level MLC RRAM of the proposed MLC-nvSRAM cell. Precharging restore scheme is employed to reduce the restore energy by suppressing the short-circuit and leakage currents when power supply is ramping up for data restore. Optimization method of multiple resistance states is also developed to maximize the restore yield considering the CMOS and RRAM process variations. The store and restore energy of the proposed MLC-nvSRAM circuit are reduced by 53.97% and 62.61%, respectively, as compared to the lowest store and restore energy of the previously published nvSRAM circuits based on single-level cell (SLC) RRAMs.**

***Index Terms*—nonvolatile SRAM, multi-level cell, RRAM, store energy, restore energy, restore yield, break-even time.**

I. INTRODUCTION

High energy efficiency is crucial for frequent-off and instant-on applications, such as battery-powered mobile devices and sensor nodes. The nonvolatile SRAM saves energy by powering down the power-hungry SRAM circuits during standby mode while storing the SRAM bit information into the nonvolatile memories with zero-standby leakage currents [1]-[3]. The resistive RAM (RRAM) devices are attractive nonvolatile element candidates in nvSRAM due to the desirable characteristics such as good scalability, fast switching speed, compatibility with CMOS fabrication process, and switching capability of multiple resistance levels [4]-[6].

Several nvSRAM circuits based on the single-level cell (SLC) RRAMs (with only two resistance levels) are presented in recent literatures [1], [2] for fast bit-to-bit parallel store/restore operations. The schematics of previously published resistive nonvolatile eight-transistor-two-RRAM (Rnv8T) and seven-transistor-one-RRAM (7T1R) SLC-nvSRAM cells are shown in Figs. 1(a) and (b), respectively. The scheme of the traditional SLC-nvSRAM macro is also illustrated in Fig. 2(a). As shown in Figs. 1 and 2(a), at least one SLC RRAM is required to store the data in each SRAM cell of the previously published SLC-nvSRAM cells. Besides, high writing current is required to flip the SLC RRAMs between the low-resistance state (LRS) and high-resistance state (HRS) with full resistance swing for successful data store. The previously published Rnv8T and 7T1R SLC-nvSRAM circuits therefore suffer from large store energy induced by fully switching the big number of SLC RRAMs for data backup.

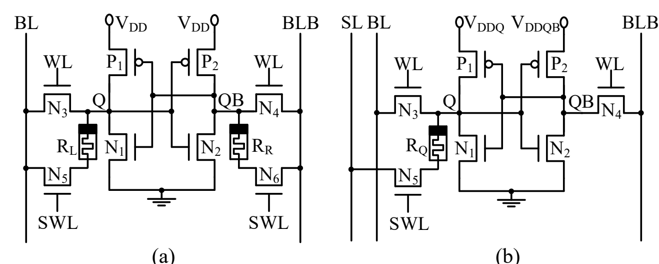

Fig. 1. Previously published SLC-nvSRAM cells. (a) Rnv8T SLC-nvSRAM cell [1]. Two SLC RRAMs (R_L and R_R) are required to back up the complementary storage data (Q and QB). N_5 and N_6 are switching transistors. *BL* and *BLB* are bitlines. *SWL* is switching line. (b) 7T1R SLC-nvSRAM cell [2]. One SLC RRAM (R_Q) is employed for data storage. *SL* is source line.

The data are recalled from the SLC RRAMs into the SRAM storage nodes in the traditional SLC-nvSRAM cells as shown in Figs. 1 and 2(a). However, large short-circuit currents are induced by two conductive paths ($P_1/R_L/N_5$ and $P_2/R_R/N_6$) for data restore when the power supply ramps up to V_{DD} in the previously published Rnv8T SLC-nvSRAM cell. Alternatively, the short-circuit currents are eliminated in the previously published 7T1R SLC-nvSRAM cell by turning off N_5 with the differential supplied initialization scheme, where V_{DDQ} is rising up (to initialize Q to a medium voltage V_{medium}, $V_{medium} < V_{DD}$) prior to V_{DDQB} [2]. However, large leakage current still exists in the inverter (P_2 and N_2) when V_{DDQB} is ramping up beyond the initialized voltage (V_{medium}) of Q in the previous 7T1R SLC-nvSRAM cell, particularly for the long ramp-up time. The previously published Rnv8T and 7T1R SLC-nvSRAM cells consequently consume high restore energy considering the long power supply ramp-up time. Therefore, reducing the store and restore energy remains a big challenge for designing high energy-efficient nvSRAM circuits.

To lower the store and restore energy with enhanced energy efficiency, a novel MLC-nvSRAM scheme utilizing the multi-level resistance characteristics of RRAM devices is proposed in this brief. The proposed MLC-nvSRAM macro is illustrated in Fig. 2(b). As shown in Fig. 2(b), *n*-bit information of successive *n* SRAM cells are stored into a single 2^n-level MLC RRAM in the proposed MLC-nvSRAM scheme.

This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grant No. 61704104, Shanghai Sailing Program under Grant No. 17Z111260004, and National Key R&D Program of China under Grant No. 2016YFB0200205.

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Alternatively, the data are recalled from the MLC RRAM into the *n*-bit SRAM cells by comparison with (2^n-1) reference resistances. In this study, *n* is assumed to be 2 for manufacturability with current processing technologies [6], [7].

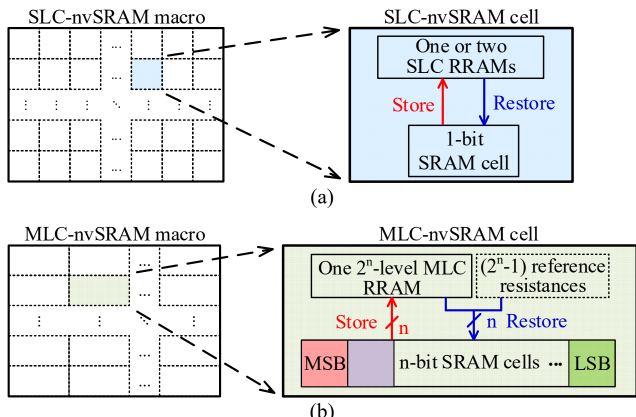

Fig. 2. Block diagrams of nvSRAM macros. (a) The traditional SLC-nvSRAM macro. (b) The proposed MLC-nvSRAM macro.

The data store circuitry is designed to enable the logic state storage of every two SRAM cells into a single four-level MLC-RRAM in this brief. The required number of switched RRAMs dedicated for data storage in the proposed MLC-nvSRAM array is reduced by more than half as compared with the previously published Rnv8T and 7T1R SLC-nvSRAM designs. Due to the less writing operations and smaller resistance swing between successive resistance states, the store energy of the proposed MLC-nvSRAM circuit is reduced by 76.80% and 53.97% as compared to the previous Rnv8T and 7T1R SLC-nvSRAM circuits, respectively. By employing the precharging restore scheme, the proposed MLC-nvSRAM cell also saves 99.91% and 62.61% restore energy, respectively, as compared to the Rnv8T and 7T1R SLC-nvSRAM cells assuming a V_{DD} ramp-up time of 10µs. Furthermore, optimization method of multiple resistance states is developed in this brief to guarantee high restore yield by considering the process variations of CMOS transistors and RRAM devices.

The brief is organized as follows. The multi-level resistance characteristics of RRAM devices are introduced in Section II. The novel MLC-nvSRAM design is presented in Section III. The proposed MLC-nvSRAM and previously published SLC-nvSRAM circuits are characterized and compared in Section IV. Finally, some conclusions are provided in Section V.

II. Multi-Level Resistance Characteristics of RRAM

The multi-level resistance characteristics of the bipolar MLC RRAMs are presented in this section. The RRAM device is a two-terminal variable resistor with an oxide layer sandwiched between the top metal electrode (TE) and bottom metal electrode (BE) as shown in Fig. 3(a). The resistance switching mechanism of a RRAM device relies on the growth/dissolution of the conductive filament which is determined by the polarity of applied voltage across the TE and BE [4].

High storage density can be achieved by employing a MLC RRAM to store multiple bits of logic states. The MLC RRAM is initially reset to HRS and then set to multiple LRS levels by tuning the compliance current (I_c) [6], [7]. I_c can be adjusted by varying the wordline (*WL*) bias voltage (V_{WL}) in the 1T1R structure as shown in Fig. 3(a). The current curves of four-level MLC RRAM with different bitline voltages (V_{BL}) are shown in Fig. 3(b). HSPICE simulation is performed with the physics-based RRAM Verilog-A model [8] and TSMC 65nm technology. Three LRS levels (LRS_1~LRS_3) are achieved by applying corresponding V_{WL} as illustrated in Fig. 3(b).

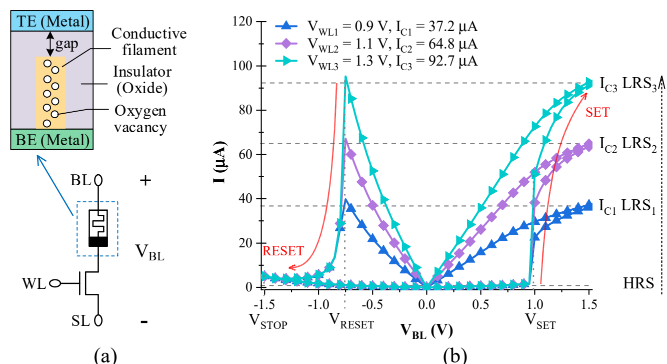

Fig. 3. (a) 1T1R device structure, consisting of one transistor and one RRAM [4]. (b) The switching curves of absolute current (I) flowing through the four-level RRAM at different bitline voltages (V_{BL}) and wordline bias voltages (V_{WL}).

III. Proposed MLC-nvSRAM Cell Design

A new MLC-nvSRAM cell for achieving low store and restore energy is proposed in this section. The schematic of the proposed MLC-nvSRAM cell is shown in Fig. 4. The 2-bit SRAM data (Q_1 and Q_2) of two SRAM cells represent the most significant bit (MSB) and least significant bit (LSB), respectively. The 2-bit data 'Q_1Q_2' are flushed into a single MLC RRAM (R_S), through the data store circuitry as shown in Fig. 4. Alternatively, the logic states are recalled from R_S and restored into the SRAM cells through two restore reference circuitries. The reference RRAM devices (R_{r1}, R_{r2}, and R_{r3}) provide three fixed reference resistances to distinguish four different logic levels. Note that, R_{r1}~R_{r3} only need to be initialized once and do not incur writing power afterwards. The foot transistors (N_{19} and N_{20}) are added in the SRAM cores and conditionally switched off for robust data restore. The normal, store, and restore modes of the new MLC-nvSRAM circuit are described in Sections III-A to III-C, respectively. Optimization method of multiple resistance states for maximizing the restore yield of MLC-nvSRAM cell is presented in Section III-D.

A. Normal Mode

The normal mode when the proposed MLC-nvSRAM circuit performs SRAM read/write operations is introduced in this section. N_{19} and N_{20} are turned on by applying high control signals (*$CTRL_1$* and *$CTRL_2$*). The voltages on the column virtual ground lines (*C_VGND_1* and *C_VGND_2*) are maintained at ~V_{GND}. The switching transistors (N_5, N_6, N_{11}, and N_{12}) are turned off with grounded restore signals (*$RSTR_1$* and *$RSTR_2$*) to disconnect the RRAMs from the storage nodes. The store signals (*STR_1* and *STR_2*) are grounded while the reset enable signal (*RST_EN*) is gated high to disable the data store circuitry. The set-line (*SL*) and reset-line (*RL*) are both 0V to suppress the leakage currents of memory array. The MLC-nvSRAM cell therefore operates like the conventional 6T SRAM cell with high data access speed.

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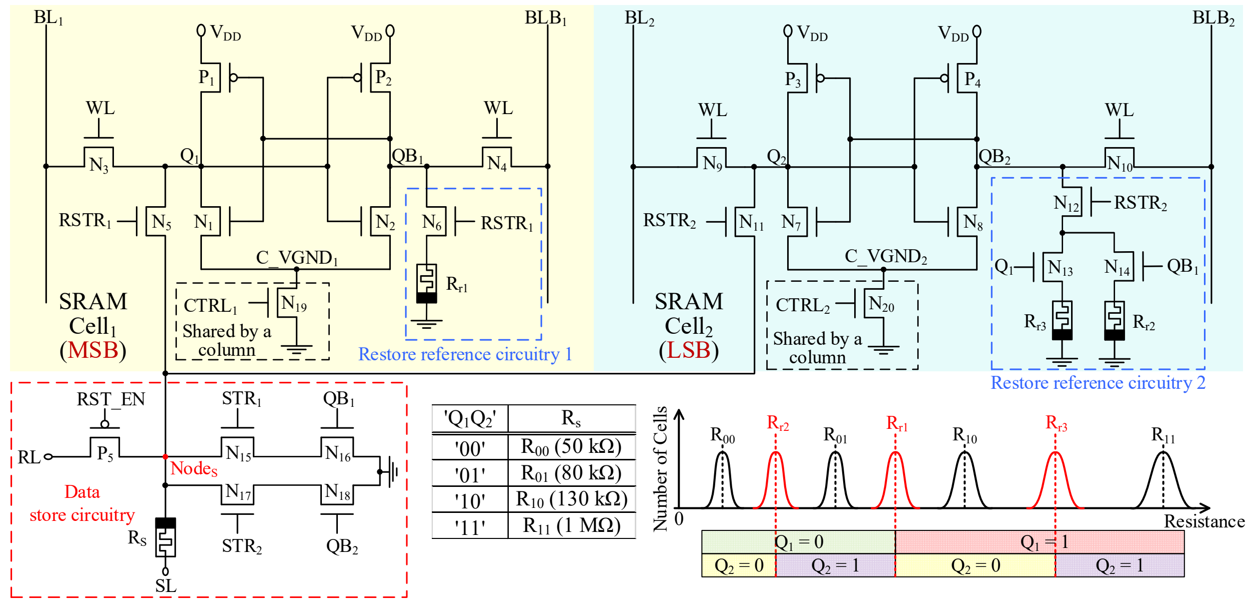

Fig. 4. Schematic of the proposed MLC-nvSRAM cell. C_VGND_1 and C_VGND_2 are shared by each column. The relationship between the resistance states of R_S and 'Q_1Q_2' is listed in the inserted table. The resistance distributions of R_S, R_{r1}, R_{r2}, and R_{r3} to distinguish 'Q_1Q_2' are also illustrated in the inserted figure.

B. Store Mode

In store mode, the 2-bit SRAM data 'Q_1Q_2' are stored into R_S by two phases (RESET and SET phases) before the memory is powered off. In the RESET phase, *RST_EN*, *SL*, *STR₁*, and *STR₂* are grounded while *CTRL₁* and *CTRL₂* are kept high. P_5 is turned on. N_{15} and N_{17} are cut off. *RL* transitions to a RESET voltage ($|V_{RESET}|$). R_S is then reset to HRS by the end of the RESET phase.

Prior to the SET phase, *RST_EN* transitions to V_{DD} and *RL* transitions to 0V. P_5 is cut off. To initiate the SET phase, *SL* transitions to a SET voltage (V_{SET}). *STR₁* and *STR₂* are biased at two different store voltages (V_{store_H} and V_{store_L}), respectively. N_{15} and N_{17} are thereby turned on. R_S is then switched to the target LRS depending on the storage data QB_1 and QB_2, which control the gate terminals of N_{16} and N_{18}, respectively. Provided that 'Q_1Q_2' store '11', QB_1 and QB_2 are both 0V. N_{16} and N_{18} are cut off. R_S is therefore maintained at HRS (R_{11}) as listed in the inserted table of Fig. 4. Alternatively, if 'Q_1Q_2' store '10', QB_1 is 0V and QB_2 is high (V_{DD}). N_{16} is cut off and N_{18} is turned on. R_S is set to a LRS of R_{10} by the active current ($I_{c,10}$) flowing through N_{17} and N_{18}. Since V_{store_H} is higher than V_{store_L}, R_S is set to the lower resistance state of R_{01} by the larger current ($I_{c,01}$) through N_{15} and N_{16} when '01' are stored in 'Q_1Q_2'. Furthermore, given that '00' are stored in 'Q_1Q_2', R_S is set to the lowest resistance state of R_{00} by the active current ($I_{c,00}$) through N_{15}, N_{16}, N_{17}, and N_{18}.

Note that, the previously published Rnv8T and 7T1R SLC-nvSRAM circuits also consist of two phases (SET and RESET phases) for data backup [1], [2]. The proposed MLC-nvSRAM array therefore provides similar store speed with the previously published SLC-nvSRAM circuits.

C. Restore Mode

In restore mode, the 2-bit data are recalled from R_S and restored into the storage nodes (Q_1 and Q_2) by experiencing three phases: precharging phase, MSB restoring phase (restoring Q_1 and QB_1), and LSB restoring phase (restoring Q_2 and QB_2). In precharging phase, the precharging restore scheme [9] is employed in this study for enhancing the restore yield and robustness against CMOS transistor variations. *STR₁*, *STR₂*, *RSTR₁*, and *RSTR₂* are maintained at 0V. *CTRL₁* and *CTRL₂* are kept low. The power supply is raising up while both *BL* and *BLB* are gradually charged to V_{DD}. All of the storage nodes (Q_1, QB_1, Q_2, and QB_2) are precharged to V_{DD} regardless of the CMOS process variations, by applying a sufficiently high voltage on *WL*. Note that, the switching transistors (N_5, N_6, N_{11}, and N_{12}) are cut off to eliminate the short-circuit currents in precharging phase. The leakage currents are also suppressed by turning off the foot transistors (N_{19} and N_{20}) during V_{DD} ramp-up period.

To initiate the MSB restoring phase, *WL* transitions to 0V and *RSTR₁* transitions to V_{DD}. N_5 and N_6 are turned on. Q_1 and QB_1 start to be discharged through two differential sensing paths (N_5/R_S and N_6/R_{r1}), respectively. Depending on the resistance difference between R_S and R_{r1}, different voltage values are restored in Q_1 and QB_1. A lower R_S induces a larger discharge current through N_5 and R_S, thereby restoring a lower voltage on Q_1. The voltages of Q_1 and QB_1 are then amplified to 0V and V_{DD}, respectively, by the cross-coupled inverters when *CTRL₁* transitions to V_{DD} and *RSTR₁* transitions to 0V. Similarly, if R_S is higher than R_{r1}, the MSB storage data (Q_1 and QB_1) are restored to V_{DD} and 0V, respectively.

Prior to the LSB restoring phase, *RSTR₂* transitions to V_{DD}. N_{11} and N_{12} are turned on. Provided that '1' (or '0') is stored on Q_1, N_{13} (or N_{14}) is turned on and R_{r3} (or R_{r2}) is chosen as the reference resistance for the comparison with R_S. Similar to the restore analysis for Q_1 and QB_1, the LSB storage data (Q_2 and QB_2) are restored depending on the resistance difference between R_S and R_{r3} (or R_{r2}). The voltages of Q_2 and QB_2 are amplified to the full swing when *CTRL₂* and *RSTR₂* transition to V_{DD} and 0V, respectively. Considering the prolonged power supply wakeup ramp at large memory subsystem level, the restore latencies of the proposed MLC-nvSRAM and previously published Rnv8T and 7T1R SLC-nvSRAM circuits are primarily determined by the V_{DD} ramp-up time [10].

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D. Optimization Method of MLC Resistance States for High Restore Yield

The resistance variations of RRAM devices in differential sensing schemes influence the sensing margins and restore yield of nvSRAM circuit [1]. To achieve reliable restore operation, the resistance allocations of multi-level RRAM (R_S) in the proposed MLC-nvSRAM cell are optimized in this section. A larger resistance ratio of two RRAMs in the differential sensing scheme leads to a larger sensing margin with enhanced restore yield [1]. Considering all the data restore scenarios for the whole range of resistance distributions as shown in Fig. 4, the minimum ratio of two successive resistance states of R_S should be maximized to achieve the highest restore yield. The objective function to be maximized can be therefore expressed as follows

$$\text{maximize}\left[\min\left(\frac{R_{01}}{R_{00}},\frac{R_{10}}{R_{01}},\frac{R_{11}}{R_{10}}\right)\right]. \tag{1}$$

Note that, the current ($I_{c,00}$) of R_S for storing '00' is the sum of the current ($I_{c,01}$) for storing '01' and the current ($I_{c,10}$) for storing '10' in store mode according to Section III-B. Besides, the resistance value of LRS is approximately inversely proportional to the current (I_c) of an MLC RRAM [11]. The relationship between R_{00}, R_{01}, and R_{10} is therefore

$$\frac{1}{R_{00}}=\frac{1}{R_{01}}+\frac{1}{R_{10}}. \tag{2}$$

The objective function in (1) is subject to (2). Assume that the minimum resistance (R_{00} = 50kΩ) and the maximum resistance (R_{11} = 1MΩ) [5] are given for all the RRAM devices. From (1) and (2), R_{01} and R_{10} are approximately equal to 80kΩ and 130kΩ, respectively.

IV. Comparison of the Proposed MLC-nvSRAM and Previously Published SLC-NvSRAM Circuits

The electrical characteristics of the proposed MLC-nvSRAM and previously published SLC-nvSRAM circuits are compared in this section. HSPICE simulation [8] is performed at 25°C. The power supply voltage (V_{DD}) is 1.2V. The widths of foot transistors in the proposed MLC-nvSRAM cell that are shared by each array column are assumed to be eight times of the minimum width with TSMC 65nm technology. The remaining transistors in all the nvSRAM cells are assumed to be minimum sized. The 3σ variations of transistor threshold voltages and RRAM resistances are assumed to be 3% and 10%, respectively, with respect to the corresponding nominal values under Gaussian distributions [12]. Considering the parasitic capacitances on internal nodes, the reference resistances in the proposed MLC-nvSRAM cell are adjusted individually to achieve 100% restore yield based on 1000 Monte-Carlo simulations for each data storage scenarios. The optimized R_{r1}, R_{r2}, and R_{r3} are equal to 55kΩ, 30kΩ, and 242kΩ, respectively, in this study. The medium voltage (V_{medium}) in the previously published 7T1R SLC-nvSRAM cell is also adjusted to be 0.9V for achieving 100% restore yield while maintaining low leakage currents in restore mode.

A. Design Metrics in Normal Mode

The design metrics of different nvSRAM circuits in normal mode and the conventional 6T SRAM circuit are evaluated in this section. As listed in Table I, the read static noise margin (*SNM*), write voltage margin, read delay, and read/write energy of the proposed MLC-nvSRAM circuit are similar (within 4% difference) to the previously published 7T1R SLC-nvSRAM and conventional 6T SRAM circuits. Alternatively, the read delay, read energy, and write energy of the proposed MLC-nvSRAM circuit are reduced by 15.53%, 25.98%, and 41.75%, respectively, due to the reduced parasitic capacitances on bitlines as compared to the previous Rnv8T SLC-nvSRAM circuit. The write delay of the proposed MLC-nvSRAM circuit is increased by up to 39.56% as compared with the previous Rnv8T and 7T1R SLC-nvSRAM circuits due to the extra load capacitances on data storage nodes. As the write delay is shorter than the read delay as listed in Table I, the slow write operation does not degrade the clock frequency of the MLC-nvSRAM circuit in normal mode. Due to the additional CMOS transistors in store and restore reference circuitries, the leakage power consumption and layout area of the proposed MLC-nvSRAM array are increased by up to 17.05% and 76.86%, respectively, as compared to the previously published Rnv8T and 7T1R SLC-nvSRAM arrays as listed in Table I.

TABLE I
Comparison of Design Metrics of NvSRAM Arrays (64 × 128-bit) in Normal Mode (TSMC 65nm CMOS Technology). V_{DD} = 1.2V.

Memory Arrays	SLC-nvSRAM		**Proposed MLC-nvSRAM**	6T SRAM
	Rnv8T [1]	7T1R [2]	**This Work**	
Read SNM (mV)	170.90	170.90	**176.90**	170.90
Write Voltage Margin (mV)	431.80	397.90	**399.60**	397.90
Read Delay (ps)	310.30	260.50	**262.10**	260.30
Write Delay (ps)	18.63	19.97	**26.00**	19.85
Read Energy (pJ)	1.27	0.94	**0.94**	0.91
Write Energy (pJ)	2.85	1.65	**1.66**	1.62
Leakage Power* (μW)	1.04	0.88	**1.03**	0.74
Array Layout Area (mm^2)	0.0166	0.0134	**0.0237**	0.008

*The average leakage power consumptions are evaluated with two different data storage scenarios (Q = '0' and Q = '1').

B. Design Metrics in Store and Restore Modes

The store energy, restore energy, and break-even times (*BET*) of the proposed MLC-nvSRAM cell and the previously published SLC-nvSRAM cells are compared in this section. For fair comparison with the proposed MLC-nvSRAM cell that contains two SRAM bits, the store and restore energy are evaluated for two SLC-nvSRAM cells. The average values of store and restore energy are reported and listed in Table II by considering all the data switching scenarios for different nvSRAM cells.

In store mode, the numbers of RRAMs required to be switched are increased in the previously published Rnv8T and 7T1R SLC-nvSRAM cells as compared to the proposed MLC-nvSRAM cell as discussed in Section I. Furthermore, high writing currents are induced when the SLC RRAMs are switched by full resistance swing or even remained at LRS in the previously published SLC-nvSRAM cells. The store energy

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of the proposed MLC-nvSRAM cell is therefore reduced by 76.80% and 53.97%, respectively, as compared to the previously published Rnv8T and 7T1R SLC-nvSRAM cells.

In restore mode, the previously published Rnv8T nvSRAM cells suffer from large short-circuit currents as discussed in Section I. High leakage current is also incurred in the 7T1R nvSRAM cells during V_{DD} ramp-up period. Alternatively, the short-circuit currents are eliminated while the leakage currents are well suppressed in the proposed MLC-nvSRAM cell by turning off the restore switching transistors and foot transistors during the precharging phase as presented in Section III-C. Assuming a V_{DD} ramp-up time (T_{ramp}) of 10μs [2] at large memory subsystem level, the restore energy of the proposed MLC-nvSRAM cell is therefore reduced by 99.91% and 62.61%, respectively, as compared to the previously published Rnv8T and 7T1R SLC-nvSRAM cells as listed in Table II.

TABLE II
COMPARISON OF DESIGN METRICS OF NVSRAM CELLS IN STORE AND RESTORE MODES. T_{RAMP} = 10μs.

nvSRAM Cells	Two SLC-nvSRAM Cells		**Proposed MLC-nvSRAM Cell**
	Rnv8T [1]	7T1R [2]	**This Work**
Store Energy (pJ)	1.25	0.63	**0.29**
Restore Energy (fJ)	14994.00	37.66	**14.08**
Sum of Store and Restore Energy (pJ)	16.24	0.67	**0.30**
Break-Even Time (ms)	2209.52	91.16	**40.82**

To characterize the overall energy efficiency of nvSRAM cells, the break-even time is evaluated next. *BET* is defined as the power off-on energy (the sum of store and restore energy) of one nvSRAM cell divided by the leakage power consumed by the conventional 6T SRAM cell at the data retention voltage (which is 0.35V in this study) [2]. As listed in Table II and shown in Fig. 5, *BET* of the proposed MLC-nvSRAM cell is reduced by 98.15% and 55.22%, respectively, as compared to the previously published Rnv8T and 7T1R SLC-nvSRAM cells. The proposed MLC-nvSRAM cell therefore provides the highest energy efficiency among all the nvSRAM cells that are evaluated in this study.

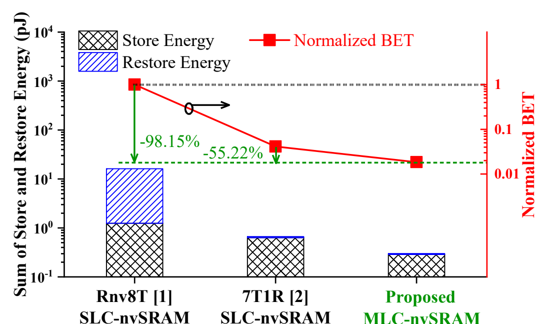

Fig. 5. Sum of store and restore energy, and the normalized (to Rnv8T SLC-nvSRAM cell) break-even times of various nvSRAM cells. T_{ramp} = 10μs.

V. CONCLUSIONS

A new nonvolatile SRAM design utilizing the multi-level cell characteristics of resistive RAMs is proposed in this brief for achieving high energy efficiency with low store and restore energy. The data store circuitry is designed to store the logic states of every two SRAM cells into a single four-level MLC RRAM. Furthermore, precharging restore scheme is employed to reduce the restore energy while enhancing the restore yield.

High data access speed is maintained with the proposed MLC-nvSRAM cell when performing the SRAM operations. The store and restore energy of the proposed MLC-nvSRAM circuit are reduced by 53.97% and 62.61%, respectively, as compared to the lowest store and restore energy of the previously published SLC-nvSRAM circuits, assuming a power supply ramp-up time of 10μs. The proposed MLC-nvSRAM circuit enhances the overall energy efficiency by providing the shortest break-even time among the nvSRAM circuits that are evaluated in this brief.

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